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Third Semester B.E. Degree Examination, Dec.2018/Jan.2019 Computer Organization

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing
ONE full question from each module.**

Module-1

- 1 a. Define the functions of following processor registers :
i) MAR ii) MDR iii) IP iv) IR. (04 Marks)
- b. How to measure the performance of a computer? Explain. (05 Marks)
- c. Compute the content of 8 bit register namely R1 and R2 containing a value of $-17_{(10)}$ and $+98_{(10)}$ with initial carry bit as 1 after performing following shift or rotate operations by 2 times. i) SHR R1, 2 ii) SAR R1, 2 [Arithmetic shift]
iii) ROR R2, 2 iv) RCR R2, 2 [Rotate right with carry]. (07 Marks)

OR

- 2 a. What is the need of processor stack? Explain a commonly used layout for information in a subroutine stack frame. (06 Marks)
- b. With relevant examples briefly explain about any 2 encoding types of machine instruction. (05 Marks)
- c. With a memory layout starting at address 'i' represent how "ABCD" data is stored in big endian and little endian assignment scheme in a system of word length 16 bits. (05 Marks)

Module-2

- 3 a. Explain how simultaneous interrupt requests from several I/O devices can be handled by processor through a single INTR line. (06 Marks)
- b. What is bus arbitration? With neat diagram explain about distributed arbitration process. (06 Marks)
- c. With a neat diagram, explain about how data is read in asynchronous bus scheme. (04 Marks)

OR

- 4 a. Explain with a neat block diagram, the hardware components needed for connecting a keyboard to a processor. (08 Marks)
- b. With a neat sequence diagram explain the process of, how output operation is carried between processor and output device connected to host through USB hub. (08 Marks)

Module-3

- 5 a. With a neat diagram, explain the design of $2M \times 32$ memory module using $1M \times 8$ memory chips. (07 Marks)
- b. Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and it consists of 4K blocks. How many bits are there in each of Tag, block/set and word fields for different mapping techniques? (09 Marks)

OR

- 6 a. Explain the process of address translation with a neat diagram. (06 Marks)
 b. With a neat diagram discuss about organization of magnetic disk. (06 Marks)
 c. Calculate the average access time experienced by processor if miss penalty is 17 clock cycles and Miss rate is 10% and cache access time is 1 clock cycle. (04 Marks)

Module-4

- 7 a. Design and explain the working of 16 bit carry look ahead adder built from 8 bit carry look ahead adder. Compare its performance with 16 bit ripple carry adder built from 8 bit ripple carry adder. (10 Marks)
 b. Calculate the product of $-2_{(10)}X + 14_{(10)}$ using bit pair recording multiplier method. Why bit pair method is better than Booth algorithm? (06 Marks)

OR

- 8 a. Perform the non restoring division for the given binary numbers where dividend is $1011_{(2)}$ and divisor is $0101_{(2)}$ with all cycles. (08 Marks)
 b. Represent $0.0625_{(10)}$ in double precision format and calculate the decimal value of A floating point number represented in single precision format as 44900000H. (08 Marks)

Module-5

- 9 a. Write and discuss about micro-routine for complete execution of instruction Add (R1), R2 in single bus organization. (08 Marks)
 b. With a detailed block diagram explain about hardwired control unit. (08 Marks)

OR

- 10 a. With a block diagram explain briefly about an embedded processor. (06 Marks)
 b. Explain briefly about different ways of implementing multiprocessor system with supportive diagrams. (06 Marks)
 c. Write the control sequence for instruction Add R4, R5, R6 for 3 bus organization. (04 Marks)

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